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(54) **Precoded waveshaping transmitter.**

(57) A precoded waveshaping transmitter comprises a synchronous delay line circuit, a transmitter state machine and a differential current digital to analog converter. Through the provision of plurality of precoded staggered time delayed data from the combination of the delay line circuit and transmitter state machine the DAC can provide a predetermined output. In a preferred implementation, a subharmonic frequency can be maintained at least 27dB below the fundamental frequency when the PWT is driven by an all ones Manchester encoded signal.

**EP 0 673 139 A2**

The present invention relates generally to a precoded waveshaping transmitter which may be used, for example in a transceiver utilized in a local area network (LAN).

In late 1990, the IEEE, the standards body which maintains LAN standards, revised the 802.3 Ethernet specification to add the so-called 10BASE-T specification, which allows use of unshielded twisted pair as one of the media for interconnection of Ethernet nodes. Because 10BASE-T lowers the overall cost of building a local area network and provides for certain network management functions not possible with traditional thick and thin coax media, it is expected to become the predominant media in the future, with the percentage of new nodes using 10BASE-T expected to rise from about 30% in 1991 to more than 80% by 1995.

Most current designs for an Ethernet network interface card (NIC) consist of three chips: a transceiver, a Manchester encoder/decoder and the network controller. The transceiver and the encoder/decoder are connected through the Attachment Unit Interface (AUI) port, which provides a medium independent interface. When twisted-pair (TP) was first introduced as a medium for Ethernet, a technique of predistorting the wide pulse and putting it through a 7th order elliptic filter with 3db band edge at 15-20 Mhz was used to fit it into the existing jitter budget of the network. Therefore, a TP medium attachment unit is usually implemented together with a transceiver, a hybrid transmit/receive filter and a transformer.

Testing and reliability issues of the discrete hybrid filter have made the integration of the external filter an important issue. Also, to improve overall reliability and costs, integration of the transceiver, encoder/decoder, external filter and eventually the network controller has become a goal for the local area network equipment designer.

One embodiment of such a precoded waveshaping technique, disclosed by LEVEL ONE COMMUNICATIONS and Fujitsu Corp. in two papers entitled 10Mb/s 10BASE-T/AUI TRANSCEIVER WITH INTEGRATED WAVESHAPING FILTER AND DATA RECOVERY, and A HIGH INTEGRATED PRODUCT FAMILY FOR 10BASE-T APPLICATIONS, respectively includes a Manchester encoded signal at its output and does not require a typical 10BASE-T 5-7th order 15MHz elliptic passive filter. The only external components are the insertion resistors and the line isolation transformer. The waveshaping technique is based on shaping the output waveform at N times the data rate to make it appear as though it has been passed through an elliptic filter. The high frequency signal aliasing is then eliminated by a first order low-pass continuous filter. To construct the significant trailing tail effect from the previous pulses, two bits of information are used to decide the proper waveshaping. Although this prior waveshaping apparatus is an

improvement over previously known systems it has some disadvantages. This technique requires an active filter which consumes additional power and also provides additional complexity to the transmitter. An additional problem is that the conventional prior art waveshaping techniques use a 1 to  $\sqrt{2}$  transform ratio to avoid headroom problems with output of the line driver. This ratio can cause nonlinear behavior at the output due to additional harmonics on the output signal. A final disadvantage of conventional waveshaping techniques is that a certain amount of open loop gain is required at the sample frequency. Hence, the line driver circuit will be sensitive to temperature and process variations.

Accordingly, what is needed is a precoded waveshaping transmitter that reduces or overcomes the above mentioned problems associated with conventional transmitters.

The present invention provides a precoded waveshaping transmitter that includes a delay line circuit for receiving a clock signal and providing a plurality of delayed clock signals; a transmitter state machine coupled to the delay line circuit for receiving data signals and the clock signal and providing a precoded plurality of staggered time delayed data; and a digital to analog converter means for providing a predetermined output, e.g. a substantially sinusoidal output.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a precoded waveshaping transmitter in accordance with the present invention.

Figure 2 is a block diagram of a delay circuit in accordance with the present invention.

Figure 3 is a block diagram of the voltage-controlled delay cell in accordance with the present invention.

Figure 4 is a block diagram of an on-chip reset cell in accordance with the present invention.

Figure 5 shows the output waveforms for each delay line versus the input reference clock in accordance with the present invention.

Figure 6 shows a timing diagram of the operation of the precoded waveshaping transmitter of Figure 1.

Figure 7 shows a waveform of the output of the precoded waveshaping transmitter of Figure 1.

## DETAILED DESCRIPTION OF THE DRAWINGS

The present invention relates to an improvement in a transmitter utilized in a local area network. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment will be readily apparent to those skilled in the art and the generic principles here-

in may be applied to other embodiments. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

The present invention discloses a pre-coded waveshaping transmitter (PWT) that overcomes design constraints of the conventional analog signal process techniques. The scheme takes full advantage of the fact that Manchester encoded data has only two fundamental frequency components in its make up. By pre-coding this information into a pre-defined sinusoid voltage template, we can reconstruct the output waveform at 20X times the data rate to make it appear as though it had been passed through an 5-7th order passive filter. The high-frequency sampling signal aliasing is then filtered out by using an first-order RC low-pass filter. The key point to the design is to using on-chip staggering timing delay lines to drive an pre-coded non-linear full differential current DAC. This design method can be used in many applications of analog signal processing, which it is necessary to be able to realize nonlinear voltage-transfer function. This requirement can be easily achieved by simply changing the current weight inside the DAC.

To more particularly describe the features of the present invention refer now to Figure 1 which is a block diagram representation of a precoded waveshaping transmitter (PWT) 10 in accordance with the present invention. The PWT 10 comprises a high frequency synchronous delay line circuit 12, a transmitter state machine 14 coupled to the delay circuit 12, an enable state machine 16 coupled to the delay line circuit 12 and the transmitter state machine. Finally the transmitter 10 includes a differential digital to analog converter (DAC) output stage 18.

In a preferred embodiment, the high frequency synchronous delay line circuit 12 provides (ten) 10 staggered timing pulses, each staggered timing pulses evenly carries 1/10 of the total delay, and the total delay is the clock period of the precise input reference clock. In this embodiment, a 20MHz (50ns period) clock is utilized as an input, so each timing pulses in 5-ns intervals apart. A delay line circuit capable of providing such timing pulses is disclosed in copending U S patent application No. entitled, A PRECISE DELAY LINE CIRCUIT WITH PREDETERMINED RESET TIME LIMIT, filed on even date herewith, assigned to the assignee of the present application and incorporated herein by reference. The operation of a preferred embodiment of the delay line circuit is described hereinbelow in conjunction with Figures 2-5.

Figure 2 shows a block diagram representation of a preferred embodiment of a delay line circuit 100 in accordance with the present invention. The delay circuit comprises voltage-controlled delay circuit 102 coupled to a sample-and-hold and low-pass filter circuit 104. An on-chip reset limit circuit 106 is coupled

between the VCD 102 and sample and hold circuits.

Through this improved delay line circuit 100 a precise delay is provided where in both edges of the clock signal are delayed in the appropriate manner. The delay line circuit 100 also through the use of the on-chip reset limiting circuit 106 provides for a predetermined time for the reset of the delay line circuit 100 which is significantly less than that of the system reset of the integrated circuit.

To more clearly describe the operation of the above-identified delay line circuit 100 refer now to Figures 3-5 in conjunction with the following discussion.

Figure 3 shows one voltage delay cell 1020 of the delay cell circuit 100 used with the present invention. The delay cell 1020 of the present invention comprises two delay cells. In so doing, zero phase shift across the delay cell 1020 is achieved and therefore, a true timing delay of the incoming reference clock (CLK) can be achieved.

The sample-and-hold circuit 104 samples the value of the output voltage from the last delay cell 1020 at the clock phase transitions. The sample and hold circuit 104 comprises two circuits 144 that operate in parallel to provide the desired output. Each of the circuits 144 samples one of the two outputs from the delay line circuit 100 on alternate clock phases. The result of the sampled outputs are then filtered and feedback as voltage control (Vctrl) 120. If the total delay through the delay line circuit 100 (sampled at the last stage delay cell 1020) is less than the clock period, then a voltage slightly less than VDD will be sampled to the sample-and-hold circuit.

Vctrl 120 will then begin increasing to add more delay through each delay cells 1020, thereby causing the total delay through the delay line circuit 100 to increase. When the total delay from the delay line circuit 100 is equal to the reference clock period, the Vctrl 120 will reach a steady-state voltage to maintain the total delay at approximately the clock period of a reference clock.

Similarly, if the total delay from the voltage controlled delay line circuit 100 is longer than the reference clock period, then a voltage slightly above ground will be sampled to the sample-and-hold circuit 104. Vctrl 120 then begins decreasing to speed up each delay cells 1020, thereby causing the total delay through the delay line circuit 100 to decrease.

Referring now to Figure 4, a block diagram of an on-chip reset limiting circuit 106 used with the present invention is shown. The on-chip reset limiting circuit 106 comprises a reset flip-flop 202 which receives a system reset signal at the input. The system reset signal is also coupled to an input of an inverter 204. The output of the inverter 204 is coupled to a second input of the flip-flop 202. The clock signal is coupled to the clock input of D flip-flops 206 and 208 respectively. The output of flip-flop 202 is coupled to the D input

of flip-flop 206 and one of the inputs of a NAND gate 210. The output of flip-flop 206 is coupled to the D input of flip-flop 208. The Q output of flip-flop 208 is coupled to a second input of the NAND gate 210. The output of the NAND gate 210 provides the limited reset signal.

The on-chip reset circuit 106 receives the system reset signal and clock signal as inputs. The reset circuit 106 resets on a system reset transition edge for a predetermined clock period, for example, a two clock period, then the reset signal goes away while the system reset is still in the reset state. Since the system reset is much longer than two clock period required to reset the delay line circuit 100, the remaining time of the system reset will enable the delay line circuit 100 to reach its steady-state condition. It should be understood that the time period for the reset can be a variety of lengths dependent upon the number and kind of logic gates utilized.

The advantage of this reset method is that no sensing circuitry is required to monitor the delay line circuit 100 operation to issue a reset signal when the delay line operates in sub-harmonic mode. Therefore, this method of resetting is more reliable than conventional delay line circuits.

Figure 5 shows a timing diagram of such a design with CLK20 being the precise input 20MHz reference clock, DAT1-DAT10 being the 10 staggered timing pulses with a true representation of the delays. As is seen, the rising and falling edges of the delays are accurately represented. Hence, the delays are more precise than those provided by conventional delay line circuits.

The precise delay line circuit 100 herein described uses a simpler reset scheme to achieve a reset requirement needed by the delay line to operate in its fundamental mode and also to provide a true timing delay of the incoming reference clock which is desired for many applications.

Referring back to Figure 1, the transmitter state machine 14 combines the input data pattern and staggered timing pulses from the delay line circuit such that, the transmitter state machine 14 generates a output code sequence at predetermined timing intervals apart. This output code sequence are then utilized by the digital-to-analog converter (DAC) 18 to reconstruct a sinusoid-like analog waveform.

This coding scheme provides for the output codes to be generated directly from the input data and the staggered timing pulses, therefor avoiding the conventional approach which requires complex state machine and ROM due to the use of active filtering techniques. Also since the output codes are directly synchronized with the precise input 20MHz clock and the jitter-free Manchester encoded data, the output jitter from the coding scheme is minimized. The transmitter state machine can be implemented in one embodiment as a switch network arrangement.

Figure 6 shows a timing diagram of such a design with data being input data pattern, ck20(0) - ck20(9) being the 10 staggered timing pulses and out(0) - out(9) being the 10 output bit lines which are associated with the input data pattern.

The enable state machine's 16 primary functions are to enable the DAC 18 and also provide a pulse width stretch function during an end of transmission delimiter (ETD) and link pulse generation.

The DAC 18 in a preferred embodiment is a four (4) bit full differential current DAC. The DAC 18 is used to translate the digital coding information from the coding scheme output to its corresponded analog output signal. The DAC is weighted in such that every bit corresponds to a pre-assigned point on a sinusoid waveform to provide the fullest frequency spectrum. In a preferred embodiment, the current output from the DAC 18 is converted into voltage through the two resistor network 20, which provides a nominal  $\pm 2.5V$  voltage swing across the twisted-pair wire. The high-frequency sampling signal aliasing is then filtered out by using a first-order RC low-pass filter 22 which is formed by two resistors and the capacitor between them.

Figure 7 shows a timing diagram of output of the PWT circuit 10 in accordance with the present invention when the PWT circuit 10 transmits a continued 10MHz output data. As is seen the output represents close to a sinusoidal function.

The pre-coding waveshaping transmitter described here uses a simply coded scheme to achieve the required 5-7th external elliptic transmit filter. In a preferred embodiment a subharmonic frequency can be maintained at least 27dB below the fundamental frequency when the circuit is driven by all-ones Manchester encoded data in accordance with the IEEE standard 802.3 10BASE-T specification. Simulations show the jitter at zero line length and 100m to be less than IEEE standard 802.3 10BASE-T specification.

Although the present invention has been described in accordance with the embodiments shown in the figures one of ordinary skill in the art will recognize there could be variations to those embodiments and those variations would be within the spirit and scope of the present invention.

Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the present invention, the scope of which is defined solely by the appended claims.

## Claims

1. A precoded waveshaping transmitter (PWT) comprising:
  - a delay line circuit for receiving a clock signal and providing a plurality of delay clock sig-

nals;

a transmitter state machine means coupled to the delay line circuit for receiving data signals and the clock signal and transmitting a plurality of precoded staggered time delayed output data; and

a digital to analog converter (DAC) means responsive to the precoded plurality of staggered time delayed data for providing a predetermined output signal.

2. The PWT of claim 1 in which the DAC means comprises 4 bit differential current DAC.

3. The PWT of claim 1 in which the transmitter state machine means further includes enable means for enabling the transmitter state machine and stretching a pulse width of the clock signal.

4. The PWT of claim 1 in which delay line circuit further comprises:

a delay stage for receiving a clock signal, the delay stage including a plurality of delay cells, the delay cells being coupled together to provide a delayed clock signal;

a sample and hold circuit coupled to the delay stage for sampling the delayed clock signal and the clock signal to determine a phase difference therebetween; and

a reset limiting circuit coupled to the delay stage and the sample and hold circuit for receiving a system reset signal and the clock signal and for resetting at a transition edge of the system reset signal for a predetermined period of time.

5. The PWT of claim 2 in which each of the plurality of delay cells comprises first and second delay circuits.

6. The PWT of claim 3 wherein each of the plurality of delay cells comprise a zero phase shifting delay cell.

7. The PWT of claim 4 in which the reset limiting circuit further comprises:

a reset means for receiving a system reset signal;

a predetermined time period setting means coupled to the reset means for receiving a clock signal and an output signal from the reset means; and

a logic gate coupled to the reset means and the predetermined time period setting means for providing a reset signal which is limited to a predetermined time period that is less than the system reset time period.

8. The PWT of claim 4 in which the reset means

comprises a first flip-flop means.

9. The PWT of claim 4 in which the predetermined time period setting means comprises:

a second flip-flop means coupled to the first flip-flop means; and

a third flip-flop means coupled to the second flip-flop means for receiving the clock signal and receiving an output from the second flip-flop means.

10. The PWT of claim 6 in which the logic gate comprises a NAND gate.

11. The PWT of claim 2 in which the reset limiting circuit further comprises:

a first flip-flop means for receiving a system reset signal;

a second flip-flop means coupled to the first flip-flop means for receiving a clock signal and an output signal from the first flip-flop means;

a third flip-flop means coupled to the second flip-flop means for receiving the clock signal and receiving an output from the second flip-flop means;

a logic gate coupled to the first flip-flop means and the third flip-flop means for providing a reset signal which is limited to a predetermined time period that is less than the system reset time period.

12. The PWT of claim 11 in which the first flip-flop means comprises a reset flip-flop and an inverter coupled to an input of the reset flip-flop.

13. The PWT of claim 11 in which the second and third flip-flop means comprise D flip-flops.

14. The PWT of claim 11 in which the logic gate comprises a NAND gate.

15. A precoded waveshaping transmitter (PWT) comprising:

a delay line circuit for receiving a clock signal and providing a plurality of delayed clock signals, the delay line circuit further comprising a delay stage for receiving a clock signal, the delay stage including a plurality of delay cells, the delay cells being coupled together to provide a delayed clock signal; a sample and hold circuit coupled to the delay stage for sampling the delayed clock signal and the clock signal to determine a phase difference therebetween; and a reset limiting circuit coupled to the delay stage and the sample and hold circuit for receiving a system reset signal and the clock signal and for resetting at a transition edge of the system reset signal for a prede-

to the reset means and the predetermined time period setting means for providing a reset signal which is limited to a predetermined time period that is less than the system reset time period;

a transmitter state machine means coupled to the delay line circuit for receiving data signals and the clock signal and transmitting a plurality of precoded staggered time delayed output data; and

a digital to analog converter (DAC) means responsive to the precoded plurality of staggered time delayed data for providing a predetermined output signal.

16. The PWT of claim 15 in which the first flip-flop means comprises a reset flip-flop and an inverter coupled to an input of the reset flip-flop.

17. The PWT of claim 15 in which the second and third flip-flop means comprise D flip-flops.

18. The PWT of claim 15 in which the logic gate comprises a NAND gate.

19. A precoded waveshaping transmitter (PWT) comprising:

a delay line circuit for receiving a clock signal and providing a plurality of delayed clock signals, the delay line circuit further comprising a delay stage for receiving a clock signal, the delay stage including a plurality of delay cells, the delay cells being coupled together to provide a delayed clock signal, each of the plurality of delay cells comprises first and second delay circuits and each of the plurality of delay cells comprise a zero phase shifting delay cell; a sample and hold circuit coupled to the delay stage for sampling the delayed clock signal and the clock signal to determine a phase difference therebetween; and a reset limiting circuit coupled to the delay stage and the sample and hold circuit for receiving a system reset signal and the clock signal and for resetting at a transition edge of the system reset signal for a predetermined period of time, the reset limiting circuit further comprising a system reset signal, a predetermined time period setting means coupled to the reset means for receiving a clock signal and an output signal from the reset means, and a logic gate coupled

to the reset means and the predetermined time period setting means for providing a reset signal which is limited to a predetermined time period that is less than the system reset time period;

a transmitter state machine means coupled to the delay line circuit for receiving data signals and the clock signal and transmitting a plurality of precoded staggered time delayed output data; and

a digital to analog converter (DAC) means responsive to the precoded plurality of staggered time delayed data for providing a predetermined output signal.

20. The PWT of claim 19 in which the DAC means comprises 4 bit differential current DAC.

21. The PWT of claim 19 in which the transmitter state machine means further includes enable means for enabling the transmitter state machine and stretching a pulse width of the clock signal.

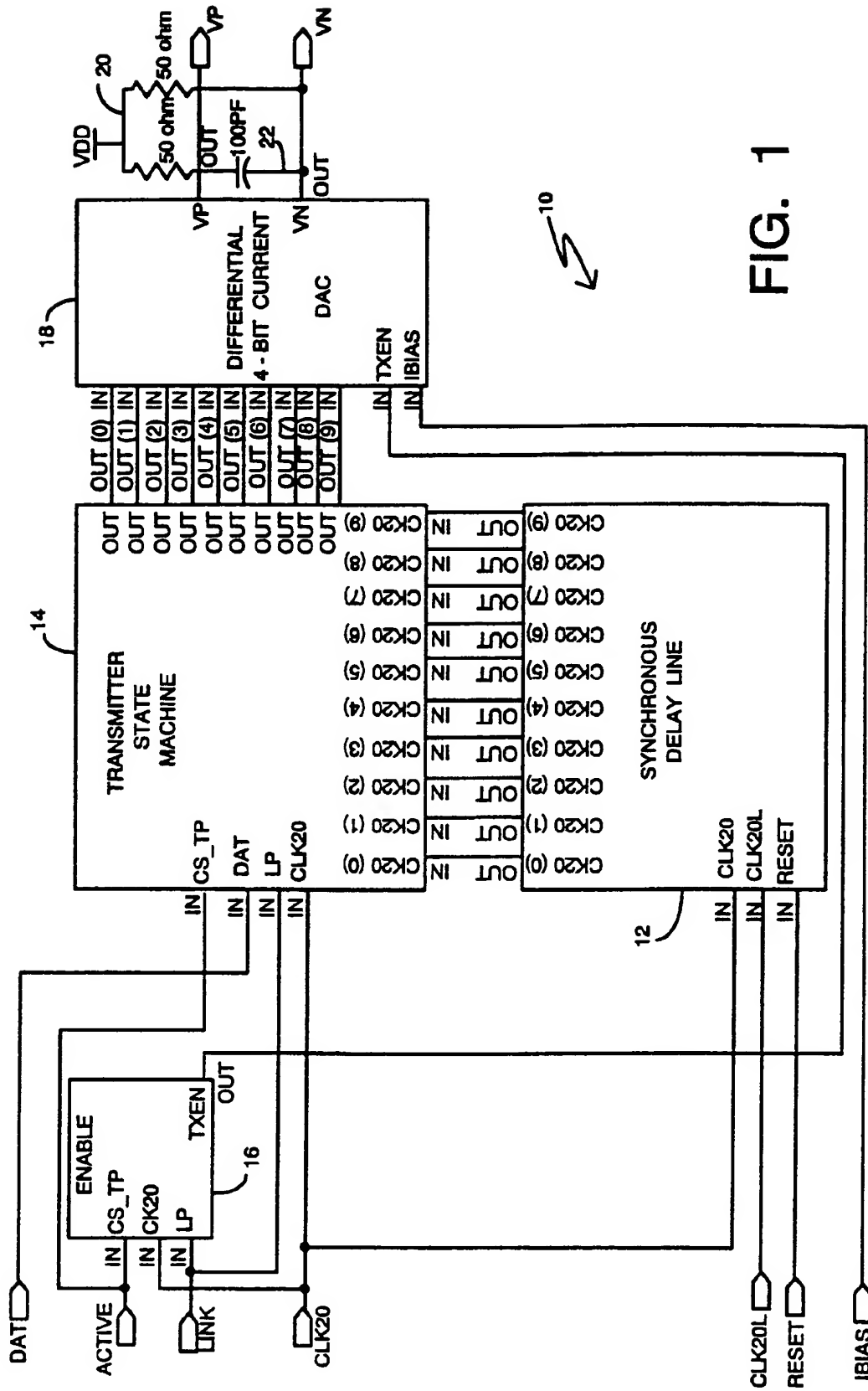


FIG. 1

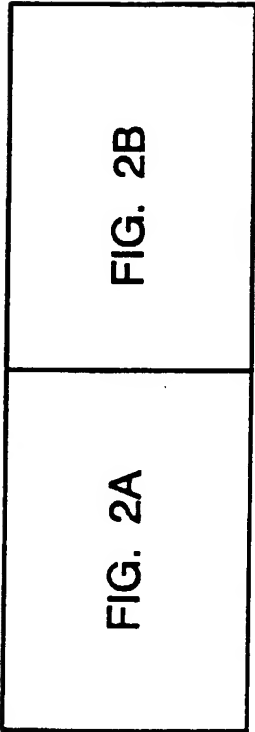


FIG. 2

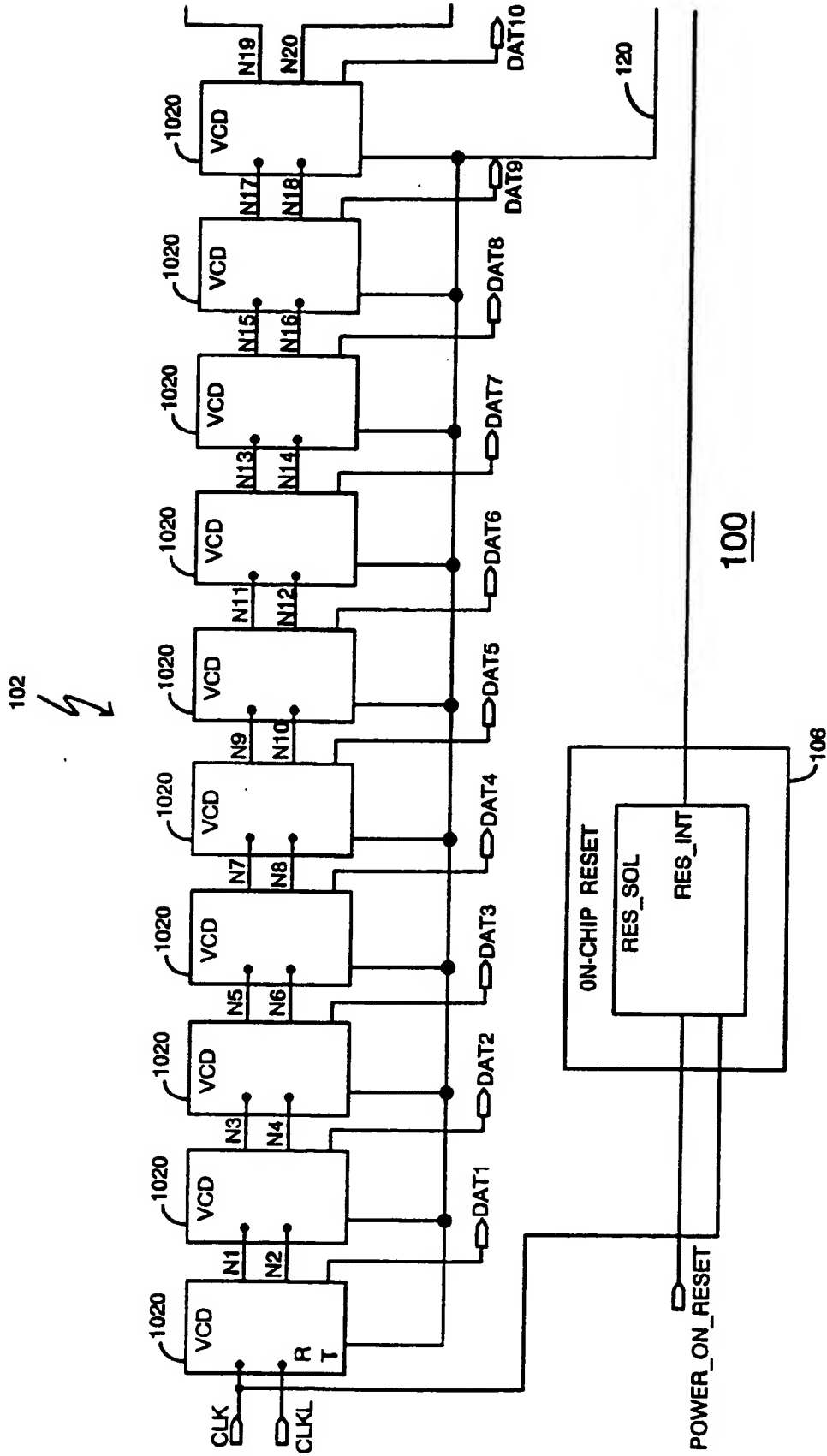


FIG. 2A

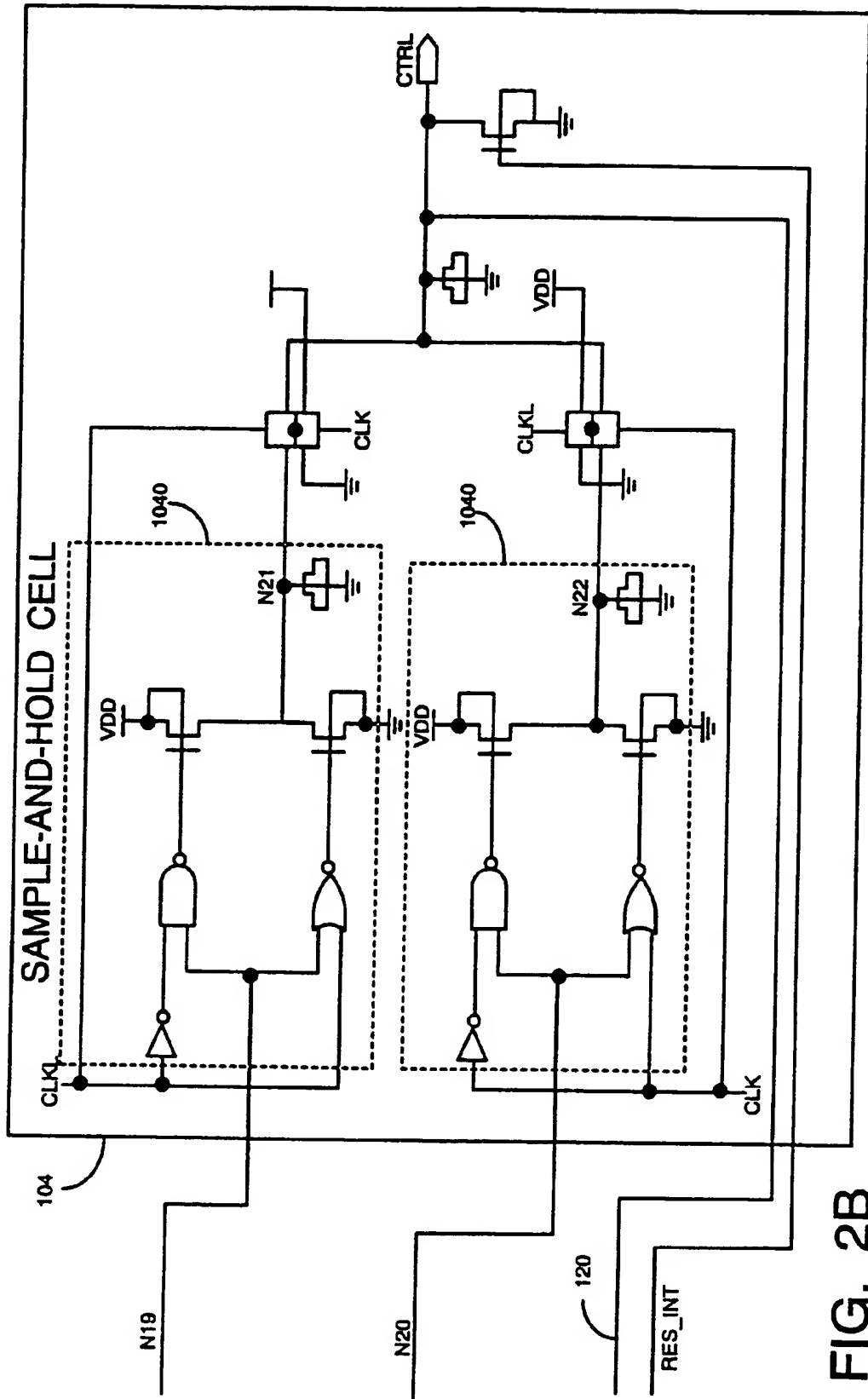
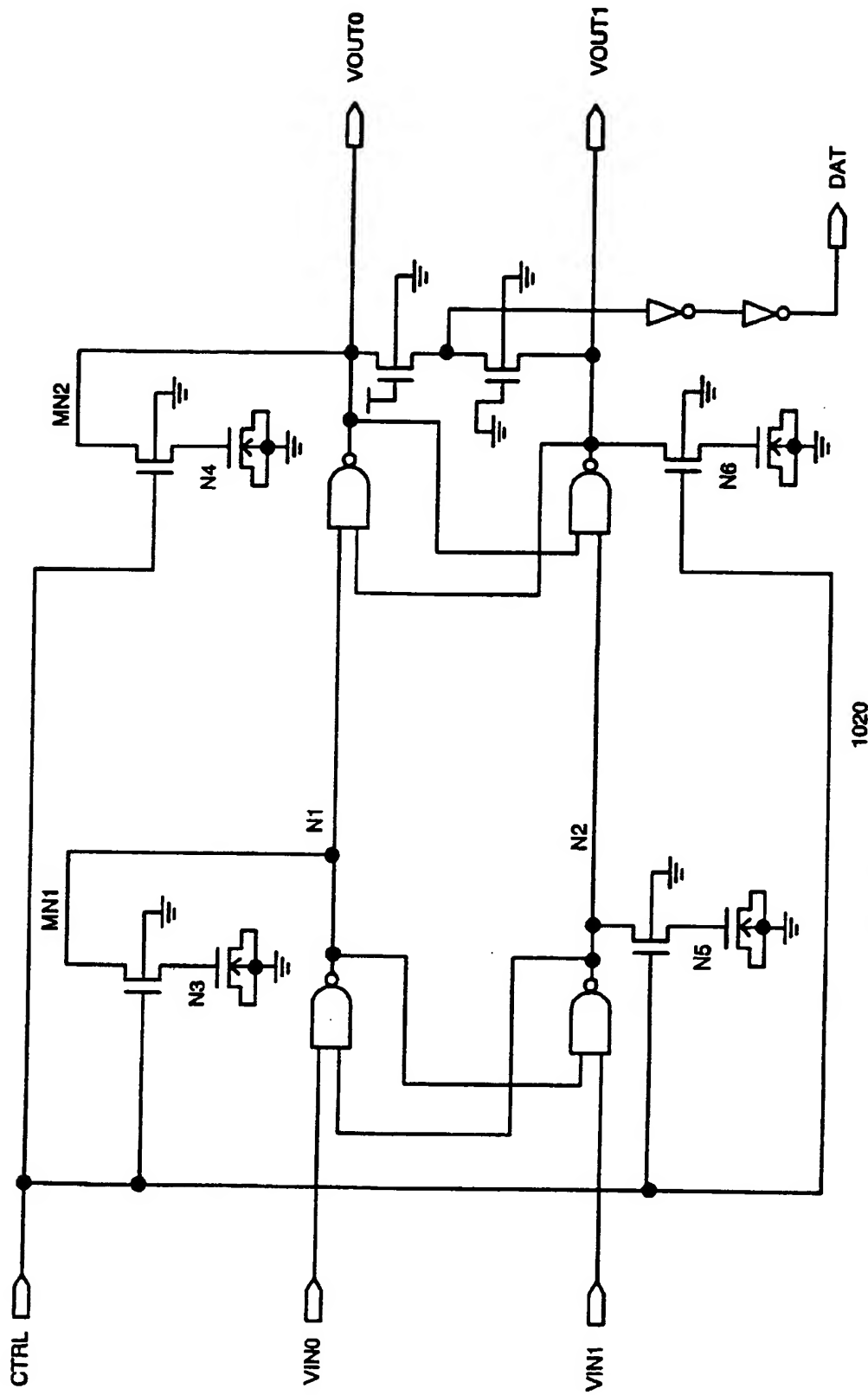


FIG. 2B



1020

FIG. 3

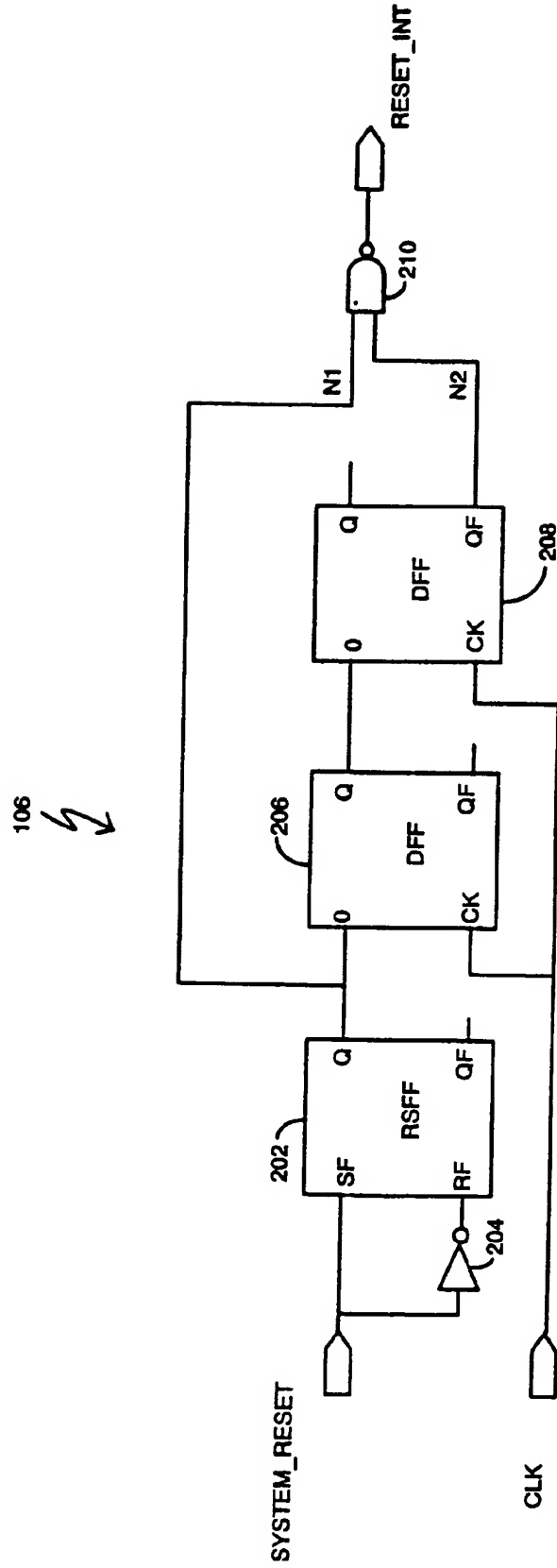


FIG. 4

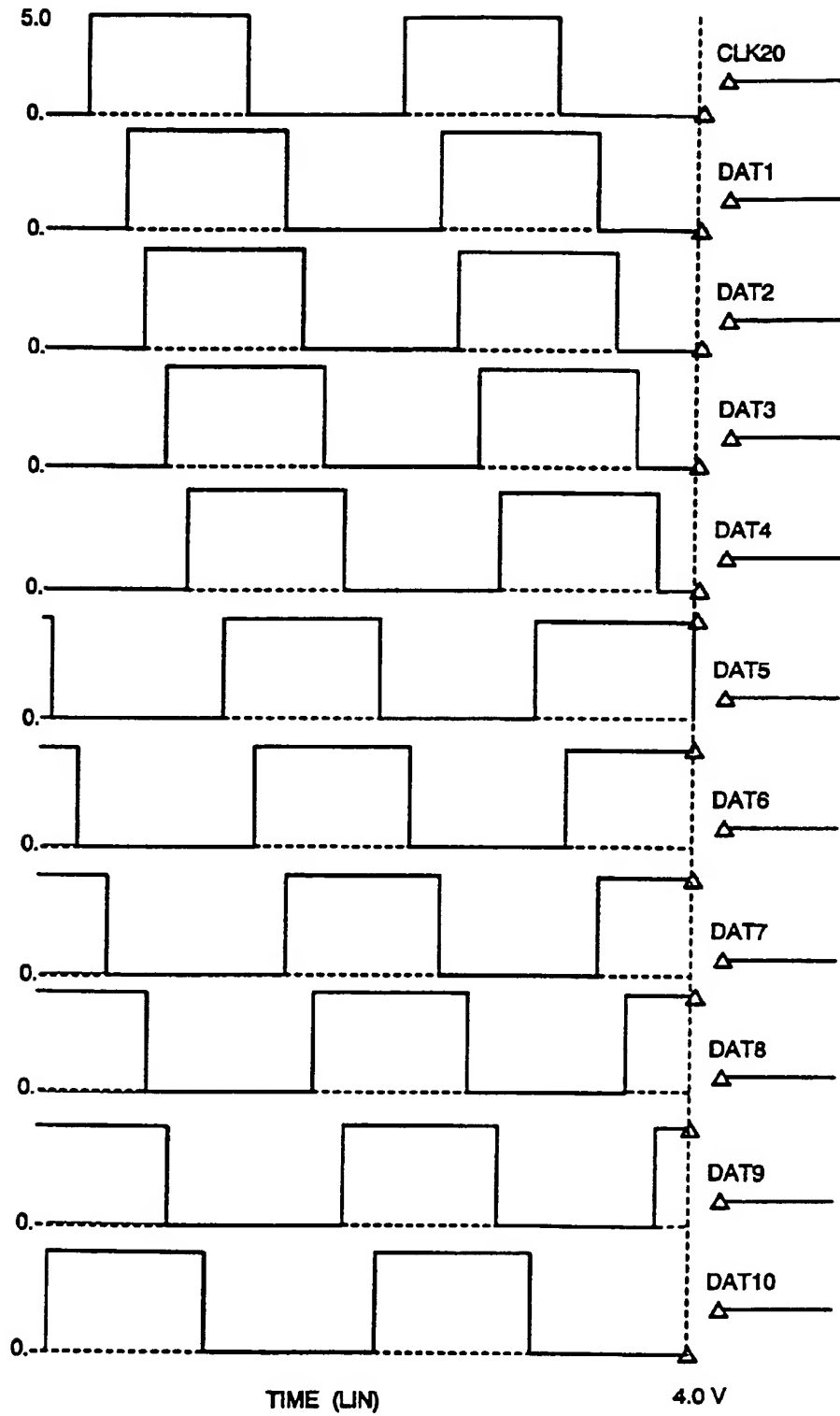


FIG. 5

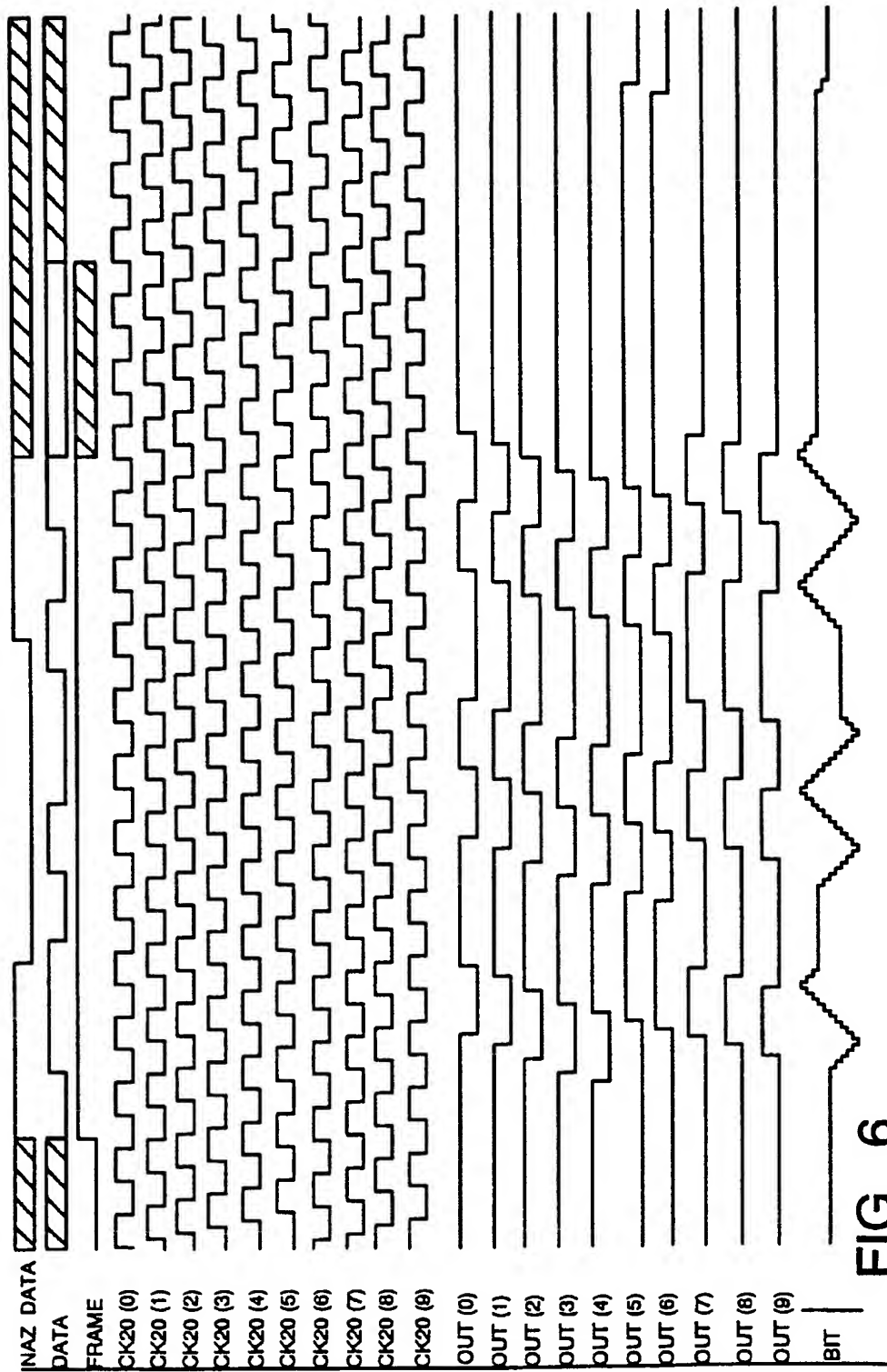


FIG. 6

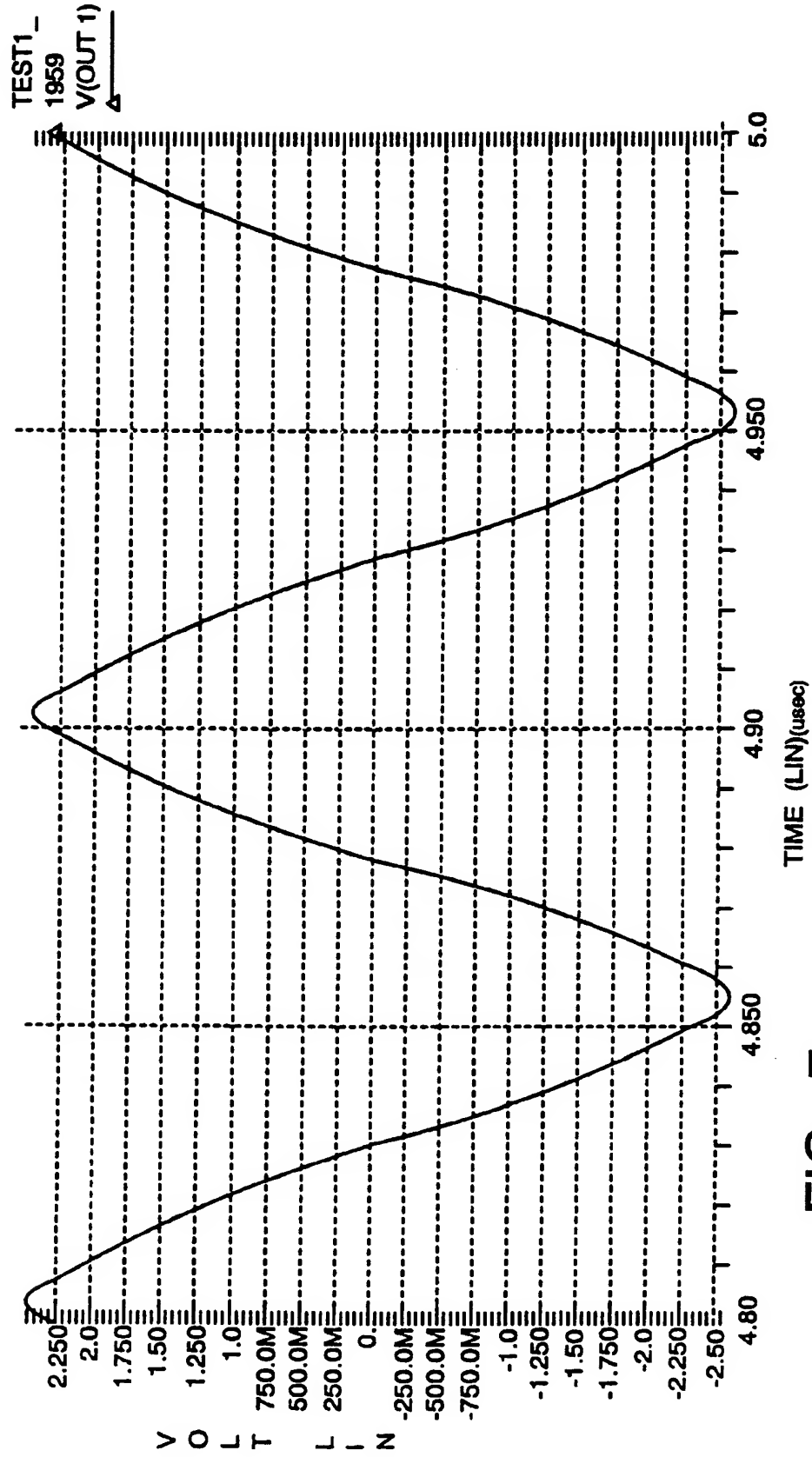


FIG. 7



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(30) Priority: **17.03.1994 US 214896**

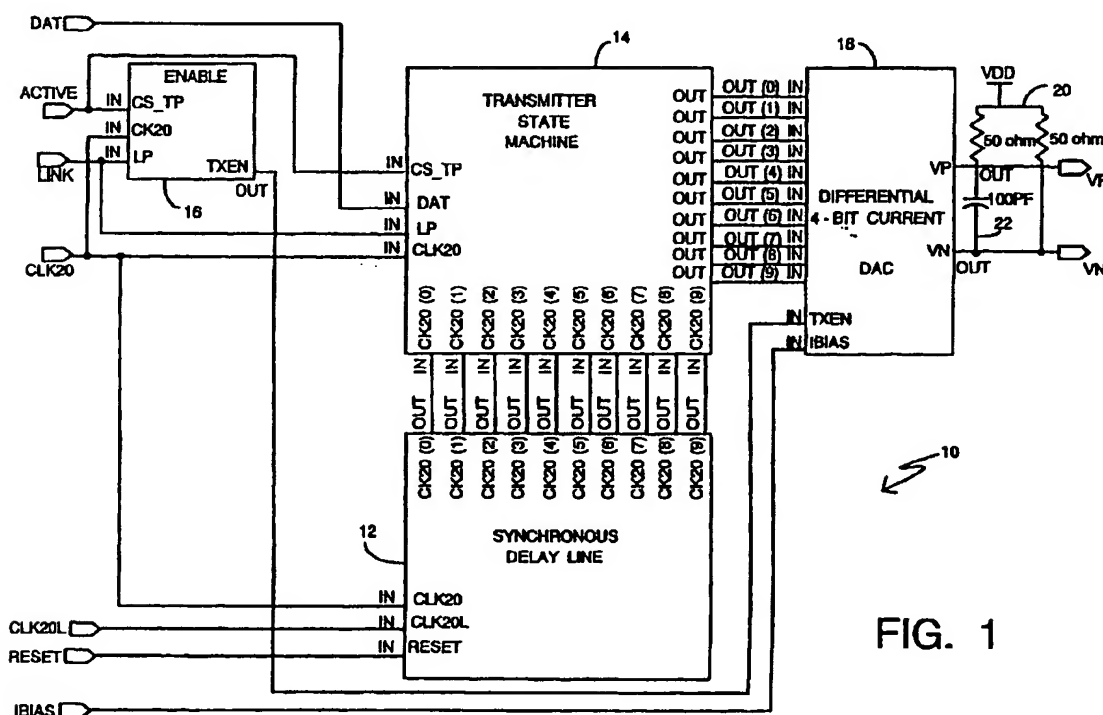
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**FIG. 1**



European Patent  
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# EUROPEAN SEARCH REPORT

Application Number  
EP 95 30 0990

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 4 975 605 A (BAZES MEL) 4 December 1990 (1990-12-04) * column 1, line 67 - column 2, line 13 * * column 2, line 20 - line 24 * * column 4, line 50 - line 52 * * column 13, line 44 - line 50 * * figures 2,14 *	1-21	H04L25/49 H04L25/03
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E	EP 0 673 117 A (ADVANCED MICRO DEVICES INC) 20 September 1995 (1995-09-20) * column 1, line 44 - line 58 * * column 8, line 45 - column 9, line 15 * * claims 1-18 * * figures 7,9 *	1-21	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H04L
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 22 September 1999	Examiner Langinieux, F
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons &amp; : member of the same patent family, corresponding document</p>			

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**ANNEX TO THE EUROPEAN SEARCH REPORT  
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EP 95 30 0990

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22-09-1999

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